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10/709,389	04/30/2004	Richard J. Grupp	BUR920040006US1	3388

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FREDERICK W. GIBB, III
GIBB INTELLECTUAL PROPERTY LAW FIRM, LLC
2568-A RIVA ROAD
SUITE 304
ANNAPOLIS, MD 21401

EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/709,389	Applicant(s) GRUPP ET AL.	
	Examiner John J. Tabone, Jr.	Art Unit 2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 and 17-30 are currently pending the application and have been examined. Claim 16 has been cancelled.

2. The Examiner has withdrawn the objections to the Specification and Claims as well as the 35 USC § 112, second paragraph rejections due to the Applicants' amendments filed 10/23/2006.

Response to Arguments

3. Applicant's arguments with respect to independent claims 1, 10, 15 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. Claim 17 is objected to because of the following informalities: This claim is improperly dependent on cancelled claim 16. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-15 and 17-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson (US007073110), hereinafter Jacobson, in view of Nadeau-Dostie et al. (US-6829730), hereinafter Nadeau-Dostie.

Claim 1:

Jacobson teaches a chip level test access port (TAP) controller having a chip-level TAP instruction register (**Host TAP 320, Fig. 3a**) and a plurality of embedded TAPs connected to said chip level TAP (**IP Core TAP 318, Fig. 3a**), said embedded TAPs having instruction register lengths that differ from said chip-level TAP instruction register, and wherein said chip level TAP includes a flexible length instruction register (**Programmable Instruction Register and Logic 304, Fig. 3a**) adapted to accommodate different length instruction registers of said embedded TAPs. Jacobson also teaches said flexible length instruction register comprises a plurality of instruction register segments (**bit registers 376, 378, . . . 380, Fig. 3c**). (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

Jacobson does not explicitly teach "at least two of said instruction register segments comprise multiple bits". However, Jacobson does teach the bit registers 376, 378, . . . 380 can be configured to programmably extend the length of the existing fixed length instruction register 182. Nadeau-Dostie teaches in an analogous art a Master TAP 100 and three embedded TAPS 102, 104 and 106, shown by dotted rectangles. Nadeau-Dostie teaches TAPs 104 and 106 are located in group 114 and have instruction registers 118 and 120, respectively, each also having three shift register elements (**at least two of said instruction register segments comprise multiple**

bits). (Fig. 3, Col. 9, l. 47 to col. 10, l. 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's bit registers 376, 378, . . . 380 to have multiple bits as in Nadeau-Dostie's embedded TAPS 102, 104 and 106. The artisan would be motivated to do so because it would enable even further flexibility in extending an existing instruction set for the boundary scan interface.

Claim 10:

Jacobson teaches a chip level test access port (TAP) controller having a chip-level TAP instruction register (**Host TAP 320, Fig. 3a**) and a plurality of embedded TAPs connected to said chip level TAP (**IP Core TAP 318, Fig. 3a**), said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other, wherein said chip level TAP includes a flexible length instruction register (**Programmable Instruction Register and Logic 304, Fig. 3a**) adapted to accommodate different length instruction registers of said embedded TAPs. Jacobson also teaches said flexible length instruction register comprises a first instruction register segment (**fixed length instruction register 382, Fig. 3c**) having a same length as a shortest embedded TAP instruction register. Jacobson also teaches said flexible length instruction register comprises a plurality of instruction register segments (**bit registers 376, 378, . . . 380, Fig. 3c**). (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

Jacobson does not explicitly teach "at least two of said instruction register segments comprise multiple bits". However, Jacobson does teach the bit registers 376, 378, . . . 380 can be configured to programmably extend the length of the existing fixed

length instruction register 182. Nadeau-Dostie teaches in an analogous art a Master TAP 100 and three embedded TAPS 102, 104 and 106, shown by dotted rectangles. Nadeau-Dostie teaches TAPs 104 and 106 are located in group 114 and have instruction registers 118 and 120, respectively, each also having three shift register elements (**at least two of said instruction register segments comprise multiple bits**). (Fig. 3, Col. 9, l. 47 to col. 10, l. 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's bit registers 376, 378, . . . 380 to have multiple bits as in Nadeau-Dostie's embedded TAPS 102, 104 and 106. The artisan would be motivated to do so because it would enable even further flexibility in extending an existing instruction set for the boundary scan interface.

In light of the combination above Jacobson in view of Nadeau-Dostie teaches <u>a second instruction register segment</u> (**bit registers 376, 378, . . . 380, Fig. 3c**) having a length equal to a difference between said shortest embedded tap instruction register and a next longer embedded TAP instruction register. (Nadeau-Dostie, col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41).

<u>Claim 15:</u>

Jacobson teaches a chip level test access port (TAP) controller having a chip-level TAP instruction register (**Host TAP 320, Fig. 3a**) and a plurality of embedded TAPs connected to said chip level TAP (**IP Core TAP 318, Fig. 3a**), said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other, wherein said chip level TAP includes a flexible length instruction

register (**Programmable Instruction Register and Logic 304, Fig. 3a**) adapted to accommodate different length instruction registers of said embedded TAPs. Jacobson also teaches a plurality of instruction register segments comprise <u>a first instruction register segment</u> comprising multiple bits (**fixed length instruction register 382, Fig. 3c**) and having a same length as a shortest embedded TAP instruction register. (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

Jacobson does not explicitly teach "at least one of said at least two other instruction register segments comprise multiple bits". However, Jacobson does teach the bit registers 376, 378, . . . 380 can be configured to programmably extend the length of the existing fixed length instruction register 182. Nadeau-Dostie teaches in an analogous art a Master TAP 100 and three embedded TAPS 102, 104 and 106, shown by dotted rectangles. Nadeau-Dostie teaches TAPs 104 and 106 are located in group 114 and have instruction registers 118 and 120, respectively, each also having three shift register elements (**at least one of said at least two other instruction register segments comprise multiple bits**). (Fig. 3, Col. 9, l. 47 to col. 10, l. 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's bit registers 376, 378, . . . 380 to have multiple bits as in Nadeau-Dostie's embedded TAPS 102, 104 and 106. The artisan would be motivated to do so because it would enable even further flexibility in extending an existing instruction set for the boundary scan interface.

In light of the combination above Jacobson in view of Nadeau-Dostie teaches <u>at least two other instruction registers segments</u> (**bit registers 376, 378, . . . 380, Fig. 3c**)

having lengths equal to a difference between a previous shorter embedded TAP instruction register and a next longer embedded TAP instruction register and said flexible length instruction register comprises a plurality of instruction register segments having a combined length equal to a longest embedded TAP instruction register and additional bit segments such that said flexible length instruction register is longer than said longest embedded TAP instruction register (Nadeau-Dostie, col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41).

Claim 22:

Jacobson teaches a chip level test access port (TAP) controller (**Host TAP 320, Fig. 3a**) and a plurality of embedded TAPs connected to said chip level TAP (**IP Core TAP 318, Fig. 3a**), said embedded TAPs have instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other, wherein said chip level TAP comprises a flexible length instruction register (**Programmable Instruction Register and Logic 304, Fig. 3a**) adapted to accommodate different length instruction registers of said embedded TAPs. Jacobson also teaches said flexible length instruction register is longer than the longest embedded TAP instruction register (**Programmable Instruction Register and Logic 304c, Fig. 3c**). Jacobson further teaches additional bit segments that are adapted to choose an effective length of said flexible length instruction register (**bit registers 376, 378, . . . 380 coupled to a selector 370, 372, . . . 374 respectively, Fig. 3c**). (Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51).

Jacobson does not explicitly teach "said flexible length instruction register comprises a plurality of instruction register segments having a combined length equal to a longest embedded TAP instruction register and additional bit segments such that said flexible length instruction register is longer than said longest embedded TAP instruction register". However, Jacobson does teach the bit registers 376, 378, . . . 380 can be configured to programmably extend the length of the existing fixed length instruction register 182. Nadeau-Dostie teaches in an analogous art a Master TAP 100 and three embedded TAPS 102, 104 and 106, shown by dotted rectangles. Nadeau-Dostie teaches TAPs 104 and 106 are located in group 114 and have instruction registers 118 and 120, respectively, each also having three shift register elements (**at least one of said at least two other instruction register segments comprise multiple bits**). (Fig. 3, Col. 9, l. 47 to col. 10, l. 17). Nadeau-Dostie also teaches adding a padding register having a length equal to the length of the instruction register of the master TAP less the length of the instruction register of the each other TAP and having an input connected to the circuit TDI, and an output (**a plurality of instruction register segments having a combined length equal to a longest embedded TAP instruction register and additional bit segments such that said flexible length instruction register is longer than said longest embedded TAP instruction register**) (Col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's bit registers 376, 378, . . . 380 to have multiple bits as in Nadeau-Dostie's embedded TAPS 102, 104 and 106. The

artisan would be motivated to do so because it would enable even further flexibility in extending an existing instruction set for the boundary scan interface.

<u>Claim 2 and 11:</u>

Jacobson teaches said flexible length instruction register is longer than the longest embedded TAP instruction register (**Programmable Instruction Register and Logic 304c, Fig. 3c**). (Col. 8, l. 49 to col. 9, l. 51).

<u>Claim 3, 12 and 17:</u>

Jacobson in view of Nadeau-Dostie teaches the flexible length instruction register further comprises additional bit segments all of said instruction register segments combined are as long as said longest embedded TAP instruction register, wherein said additional bit segments make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active segments of said flexible length instruction register (**bit registers 376, 378, . . . 380 coupled to a selector 370, 372, . . . 374 respectively, Fig. 3c**). (Jacobson, Col. 8, l. 49 to col. 9, l. 51). (Nadeau-Dostie, Fig. 3, Col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41, col. 9, l. 47 to col. 10, l. 17).

<u>Claim 4 and 23:</u>

Jacobson in view of Nadeau-Dostie teaches said plurality of instruction register segments comprises <u>a first instruction register segment</u> (**fixed length instruction register 382, Fig. 3c**) having a same length as a shortest embedded TAP instruction register and <u>a second instruction register segment</u> (**bit registers 376, 378, . . . 380, Fig. 3c**) having a length equal to a difference between said shortest embedded TAP

instruction register and a next longer embedded TAP instruction register. (Jacobson, Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51). (Nadeau-Dostie, Fig. 3, Col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41, col. 9, l. 47 to col. 10, l. 17).

Claim 5 and 24:

Jacobson in view of Nadeau-Dostie teaches said plurality of instruction register segments comprises a first instruction register segment (**fixed length instruction register 382, Fig. 3c**) having a same length as a shortest embedded TAP instruction register and at least two other instruction registers segments (**bit registers 376, 378, . . . 380, Fig. 3c**) having lengths equal to a difference between a previous shorter embedded tap instruction register and the next longer embedded TAP instruction register. (Jacobson, Col. 3, ll. 16-38, col. 7, ll. 21-64, col. 8, l. 49 to col. 9, l. 51). (Nadeau-Dostie, Fig. 3, Col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41, col. 9, l. 47 to col. 10, l. 17).

Claim 6, 18 and 25:

Jacobson in view of Nadeau-Dostie teaches selection logic connected to each of said instruction register segments and to said additional bit segments, wherein said selection logic comprises a plurality of multiplexors (**selectors 370, 372, . . . 374, Fig. 3c**) adapted to selectively include with said first instruction register segment incremental ones of said instruction register segments to incrementally match a difference in length between longer embedded TAP instruction registers said first instruction register segment. (Jacobson, Col. 8, l. 49 to col. 9, l. 51). (Nadeau-Dostie, Fig. 3, Col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41, col. 9, l. 47 to col. 10, l. 17).

Claim 7, 19 and 26:

Jacobson in view of Nadeau-Dostie teaches the effective length of said flexible length instruction register comprises a combined length of said first instruction register segment and selected ones of said at least two other instruction registers segments. (Jacobson, Col. 8, l. 49 to col. 9, l. 51). (Nadeau-Dostie, Fig. 3, Col. 3, ll. 10-14, 38-41, col. 7, ll. 36-41, col. 9, l. 47 to col. 10, l. 17).

Claim 8, 13, 20 and 27:

Jacobson teaches said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip level TAP. (Col. 8, l. 49 to col. 9, l. 51).

Claim 9, 14, 21 and 28:

Jacobson teaches selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP (**the IMUXes 316, 326 and OMUXes 316, 324 can connect to the IP processor core(s) and the JTAG TAP signals TCK 330, TDI 322, TDO 336, and TMS 332**). (Col. 7, ll. 21-40).

Claim 30:

Jacobson teaches the number of said embedded TAPs is unlimited in that the invention is not limited to the precise arrangements shown in FIG. 1. (Col. 7, ll. 38-40). Jacobson also teaches although only connections to the IP processor core IR 338 and IP processor core DR1 340 and IP processor core DR2 342 are shown, the invention is not limited in this regard. (Col. 7, ll. 44-47).

Claim 29:

Jacobson does not explicitly disclose that the "**embedded TAPs comprise serially connected TAPs**". Nadeau-Dostie illustrates in an analogous art a Master TAP 100 and three embedded TAPS 102, 104 and 106, shown by dotted rectangles. Nadeau-Dostie teaches TAPs 104 and 106 are located in group 114 and have instruction registers 118 and 120, respectively, each also having three shift register elements. Instruction registers 104 and 106 are serially connected in a serial or daisy chain (**embedded TAPs comprise serially connected TAPs**) between a group TDI node 122 and a group TDO node 124. Group 114 has the longest instruction register chain length of the embedded groups, having a total of six shift register elements or bits. (Fig. 3, Col. 9, l. 47 to col. 10, l. 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jacobson's TAP configuration with Nadeau-Dostie TAP configuration in order to serially connect IP Core TAP(s) 318. The artisan would be motivated to do so because it would enable Jacobson to serially string different embedded core TAPs 318 in order to save test time.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 1/5/07

John J. Tabone, Jr.
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100